IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. Filing Date March 27, 2000 (Aug. 17 2004) Weimin (Michael) Li Inventor Micron Technology, Inc. Group Art Unit Toniae M. Thomas

Title: Low k Interlevel Dielectric Layer Fabrication Methods

To:

Box RCE

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450 -

From:

James E. Lake

(Tel. 509-624-4276; Fax 509-838-3424)

Wells St. John P.S.

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509-624-4276

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

This Request for Continued Examination (RCE) Application is being filed in an abundance of caution to ensure consideration of the references listed on the attached form PTO-1449.

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether the submitted references are prior art.

Respectfully submitted,

Reg. No. 44,854

Form PTO-14	49		U.S.	DEPARTMENT OF COMMERCE ENT AND TRADEMACOFFICE	ATTY. DOCKET NO. SERIAL NO. 09/536,037				
		LIST OF ART CITES	AND ADDITON		APPLICANT Weimin Li, et al.				
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				NA PATENCE OCUMENTS			•		
*Examiner Initial		Document Number	Name		Class	Subclass	Filing Date If Appropriate		
	AA	6,153,504	11/2000	Shields et al					
	AB	4,971,655	Stafano et al						
	AC	6,498,084 B2	12,2002	Bergemont	-				
	AD	5,036,383	07/1991	Mori					
	AE	5,593,741	01/1997	Ikeda .					
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	1			FOREIGN PATENT DOCUMEN	TS				
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	AM	08-045926A	02/1996	Japan				Yes	No
	AN	JP8051058	02/1996	Japan					
	AO	JP63316476	12/1998	Japan	_				
	AP	JP8078322	03/1996	Japan					
	AQ	10-163083	06/199	J apan					
		(OTHER REFEREN	NCES (including Author, Title, Date	, Pertinent Pages, Etc.)				
	AR	Wolf, S., Silicon I	Processing for the	VLSI ERA. Vol. 3, The Submicro	on MOSFET p. 635	, 			
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EXAMINER	·	•		DATE CONSIDER	ED				
	*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.								

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No	09/536 037
Filing Date	March 27, 2000
nventor	Veimin (Michael) Li et al
Assignee	Micron Technology Inc
Group Art Unit	
Examiner	Toniae M. Thomas
Attorney's Docket No.	MI22-1398
Title: Low k Interlevel Dielectric Layer Fabrication Methods	

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 09/388,826, filed September 1, 1999. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2). Citation of these references is respectfully requested.

Respectfully submitted,

David G. Latwesen Ph.D.

Reg. No. 38,533

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO. MI22-1398 SERIA NO. 09/536,037

IST O	FART	CITED	BY	APPL	ICANT
(1	ise seve	ral sheets	if ne	cessary)

APPLICANT
Weimin Li, et al.
FILING DATE
March 27, 2000

GROUP 2822

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	_			U.S. PATENT DOCUMEN	TS				
*Examiner Initial		Document Number	Date	Name	в	Class	Subclass	Filing If Appr	g Date ropriate
	AA	6,503,818 B1	01/2003	Jang					
	AB	6,486,061 B1	11/2002	Xia et al.					
	AC	6,486,057 B1	11/2002	Yeh et al.	***************************************				
	AD	6,465,372 B1	10/2002	Xia et al.				,	
	AE	6,444,593 B1	09/2002	Ngo et al.					·
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	AG	6,435,943 B1	08/2002	Chang et al.			,		
	АН	6,429,115 B1	08/2002	Tsai et al.					
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	AJ	6,030,901	02/2000	Hopper et al.					
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	AL	5,994,217	11/1999	Ng					
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		Document Number	Date	Countr	y	Class	Subclass	Trans	lation
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<u>.</u>	AM	8046186	02/1996	Japan					
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Form PTO-1449

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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)

APPLICANT Weimin Li, e

					March 27, 2000	,	2822	<u> </u>	
				U.S. PATENT DOCUMENTS					
*Examiner Initial		Document Number	Date	Name		Class	Subclass	Filing If Appr	Date opriate
	AA	5,985,519	11/1999	Kakamu et al.					
	AB	5,747,388	05/1998	Küsters et al					
	AC	5,639,687	06/1997	Roman et al		-	·		
•	AD	5,498,555	03/1996	Lin			·		
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	AP						·		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No	
Filing Date	March 27, 2000
Inventor	Weimin Li
Assignee	Micron Technology, Inc.
Group Art Unit	2822
Examiner	T. Thomas
Attorney Docket No.	
Title: Low k Interlevel Dielectric Layer F	abrication Methods

Commissioner for Patents P.O. Box 1450 Art Unit 2822 Alexandria, VA 22313-1450



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Supplemental Information Disclosure Statement; PTO-1449

Gail Wright

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No	
Filing Date	
Inventor	
Assignee	Micron Technology, Inc.
Group Art Unit	
Examiner	T. Thomas
Attorney Docket No	
Title: Low k Interlevel Dielectric Laver Fa	

Commissioner for Patents P.O. Box 1450 Art Unit 2822

Alexandria, VA 22313-1450

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Dated: 12/2004

Gail Wright

Telephone No.

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PTO/SB/21 (02-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 2 hours to complete, including getnering, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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